REMARKS

This Response is intended as a complete response to the Final Office Action dated July 27, 2006. In view of the following discussion, the Applicants submit that all claims are presently in condition for allowance.

CLAIM AMENDMENTS

Claim 22, although withdrawn, has been amended to reflect the subject matter of claim 1, as amended.

CLAIM REJECTIONS

35 USC §103

A. Claims 1 and 15

Claim 1 and 15 stand rejected under 35 USC §103 as being anticipated by US Patent No. 6,625,497, issued September 23, 2003, to *Fairbairn, et al.* (hereinafter *Fairbairn*) in view of US Patent Application Publication No. 2004/0078108, published April 22, 2004, to *Choo, et al.* (hereinafter *Choo*). In response, the Applicants have amended claim 1 to more clearly recite aspects of the invention.

Independent claim 1 recites limitations not taught or suggested by any combination of the cited art. *Fairbairn* teaches a semiconductor processing module with integrated feedback/feed forward metrology. Specifically, *Fairbairn* teaches reducing critical dimension (CD) variation by feeding back information gathered during inspection of a wafer (e.g., after photoresist development) to upcoming lots that will be going through the photolithography process, and by feeding forward information to adjust the next process the inspected wafer will undergo (e.g., the etch process). *Fairbairn*, col. 4, ll. 40-46. *Fairbairn* further teaches taking post-etch CD measurements and optionally reviewing the wafer if a significant variation from normal post-etch data is observed. *Id.*, col. 12, ll. 24-34; col. 13, ll. 55-65.

Choo teaches scatterometry techniques for measuring one or more dimensions of a first integrated circuit during a fabrication process. The measurements may be used feed forward or feed back information that may be utilized to adjust operating

parameters of other processing components to which the same or other die will be subjected. *See Choo*, p. 5, ¶ [0042].

However, *Choo* fails to teach or suggest a modification of the teachings of *Fairbairn* that would yield a process of measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate; adjusting a process recipe of an etch process for etching the substrate and a process recipe of at least one post-etch process using the results of measuring the dimensions on the structures; and executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established because the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Applicants submit that independent claim 1, and claim 15 depending therefrom, are patentable over *Fairbairn* in view of *Choo*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

B. Claims 2-5 ,8-14, 16-17, and 53

Claims 2-5, 8-14, 16-17 and 53 stand rejected under 35 USC §103 as being unpatentable over *Fairbairn* in view of *Choo*, and further in view of US Patent 6,567,717, issued May 20, 2003, to *Krivokapic, et al.* (hereinafter *Krivokapic*). Claim 2 has been cancelled. In view of the amendment to claim 1, from which the above rejected claims depend, the Applicants respectfully disagree.

Independent claim 1, from which claims 3-5, 8-14, 16-17 and 53 depend, recites limitations not taught or suggested by any permissible combination of the cited art. The patentability of claim 1 over the combination of *Fairbairn* and *Choo* is discussed above. *Krivokapic* is cited for the proposition that it teaches that, after a post-etch measurement, wafers may be returned for further etching if under-etched. However, *Krivokapic* merely teaches and suggests further etching of an under-etched workpiece if, and only if, the desired etch results were not obtained during a first etch, and fails to teach a multi-pass process as recited in the claims.

In the Response to Arguments section of the Final Office Action, the Examiner asserts that the CD measurement of *Krivokapic* falls within the scope of "a post etch process" as recited in the claims. The Applicants disagree. However, the Applicants have amended claim 1 to more clearly recite aspects of the invention.

Specifically, with particular respect to amended claim 1, *Krivokapic* clearly fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established because the combination of the cited references fails to yield the limitations recited in the claim.

Thus, the Applicants submit that independent claim 1, and claims 3-5 and 8-14, 16-17 and 53 depending therefrom, are patentable over *Fairbairn* in view of *Choo*, and further in view of *Krivokapic*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

C. Claims 6, 7, and 18

Claims 6, 7, and 18 stand rejected under 35 U.S.C. §103 as being unpatentable over *Fairbairn* in view of *Choo*, in further view of US Patent Application No. 2004/0087041 published May 6, 2004 to *Perry, et al.* (hereinafter *Perry*). In view of the amendment to claim 1, from which the rejected claims depend, the Applicants respectfully disagree.

Independent claim 1, from which claims 6, 7 and 18 depend, recites limitations not taught or suggested by any permissible combination of the cited art. The patentability of claim 1 over the combination of *Fairbairn* and *Choo* is discussed above.

Perry discloses a method of controlling a recess etch process. Specifically, *Perry* teaches determining the absolute vertical dimension of a column of material to be etched in a substrate (i.e., a trench) and using single- or multi-wavelength interferometry to monitor the actual etching of the recess. (*Perry*, ¶[0039].) However, *Perry* fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1.

Hence, *Perry* fails to teach or suggest a modification of *Fairbairn* and *Choo* that would yield the limitations recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Applicants submit that claims 6, 7, and 18 are patentable over *Fairbairn* in view of *Choo*, and further in view of *Perry*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

D. Claims 19-21

Claims 19-21 stand rejected under 35 U.S.C. §103 as being unpatentable over *Fairbairn* in view of *Choo*, and further in view of US Patent Application No. 2003/0022510 published January 30, 2003 to *Morgenstern* (hereinafter *Morgenstern*). In view of the amendment to claim 1, from which the rejected claims depend, the Applicants respectfully disagree.

Independent claim 1, from which claims 19-21 depend, recites limitations not taught or suggested by any permissible combination of the cited art. The The patentability of claim 1 over the combination of *Fairbairn* and *Choo* is discussed above. The Examiner cites *Morgenstern* to show a process of forming a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl_2 chemistry.

However, *Morgenstern* fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1. Hence, *Morgenstern* fails to teach or suggest a modification of *Fairbairn* in view of *Choo*, that would yield the limitations recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Applicants submit that claims 19-21 are patentable over *Fairbairn* in view of *Choo*, and further in view of *Morgenstern*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

E. Claims 36-52

Claims 36-52 stand rejected under 35 USC §103 as being unpatentable over *Fairbairn* and *Choo*, as applied to claim 1, and further in view of *Krivokapic* and *Perry*. The Applicants respectfully disagree, however, the Applicants have amended claim 36 to more clearly recite aspects of the invention.

Independent claim 36 recites limitations not taught or suggested by any permissible combination of the cited art. The Examiner admits that *Fairbairn* is silent with respect to a multi-pass process and asserts that the re-work of under etched wafers as taught by *Krivokapic* "in effect describes a multi-pass process." *Office Action*, p. 11, ll. 12-16. However, as noted above in section B, although *Krivokapic* teaches further etching of an under-etched workpiece, such re-work is not a multi-pass process as defined by the claims.

However, the Applicants have amended claim 36 to more clearly recite aspects of the invention. Specifically, with respect to amended claim 36, *Krivokapic* clearly fails to teach or suggest executing a multi-pass process, wherein the substrate is processed more than once by at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch process is a pass; and measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate, during each at least one measurement process, as recited in claim 36.

Also, as discussed above in section C, *Perry* similarly fails to teach or suggest a multi-pass process as recited in claim 36. Accordingly, *Choo*, *Krivokapic*, and *Perry* fail to teach or suggest a modification to the teachings of *Fairbairn* that would yield the limitations recited in claim 36. Therefore, a *prima facie* case of obviousness has not been established because the combination of the cited references fails to yield the limitations recited in the claim.

Thus, the Applicants submit that independent claim 36, and claims 37-52 depending therefrom, are patentable over *Fairbairn* and *Choo*, as applied to claim 1, and further in view of *Krivokapic* and *Perry*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If the Examiner believes that there are any unresolved issues, it is requested that the Examiner telephone Mr. Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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Date

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